CASE STUDY

Sarcina Delivers Right-First-Time Packages Using ADS For Chip-Package-Board Simulation

KEYSIGHT

Right-first-time IC Package Design Solution

Organization

- Sarcina Technology LLC

Challenges

- Ease of Use
- ASIC Package Design
- Dense, High-Power Devices
- Chip-Package-Board Signal Integrity > 100 Gbps

Solutions

- Advanced Design System (ADS); SI/PI Pro
- ADS Memory Designer
- IBIS-AMI Simulation Model Integration

Results

- Simulation Accuracy
- DDR6 and 112 GbE PAM-4 Package Success
- Significant Cost Savings

Semiconductor package engineering has a unique set of challenges that make it difficult for fabless semiconductor companies to win first-time success. Packages come in many different materials and topologies, suited for different applications such as medical, aerospace, automotive, consumer electronics, etc. Converging on an optimal package design for complex semiconductors such as CPU/GPU/NPU has evolved into a highly specialized practice

Sarcina Technology LLC, headquartered in Palo Alto with a presence in Taipei, Taiwan, is one such semiconductor package design services. Established in 2011, Sarcina has carved a niche in designing semiconductor packages for some of the most sophisticated devices in the market. Their prowess is showcased in their work on workstations and datacenter CPUs, GPUs, and network processors that employ the latest technologies.

As a premier "wafer-in, package-out" service provider, they adeptly incorporate the latest standards for interconnect, such as DDR6, PCIe Gen 6, SERDES, and 100 Gbps (and faster) Ethernet. Many of the semiconductor dice they cater to are true powerhouses, drawing hundreds of watts during peak operation. Packages designed by Sarcina have found their way into diverse sectors, ranging from consumer electronics to space endeavors like the Falcon 9 mission to the ISS in May 2020.

Sarcina has proven themselves by achieving first-time successful tape-out time and time again. Larry Zu, Sarcina's CEO, says the company possesses deep advanced semiconductor package design experience. Larry sheds light on the company's strategic use of Keysight's PathWave ADS for their groundbreaking chip-package-board channel simulations.

Challenge: Accurate signal path analysis

Semiconductor packages, especially those used with modern high-performance and high-bandwidth devices, form a critical part of the overall signal path. Take a high-end network processor for example, a signal comes in from an internal silicon gate, then travels along a silicon-metal transmission line, to a bump or chip bond pad, then through the package to the host motherboard. There are vias and transmission lines throughout each of these sections and transitions between them. All of these transitions and vias are opportunities for electrical signal degradation and must be optimized.

Sarcina designs the package, by analyzing the entire signal path from chip, to bump, to package, to board, to connector and all along the line to the receiving device. This adds significant complexity to the configuration of traditional SPICE-based tools, making for very slow progress. Sarcina package design methodology features full channel simulation. The challenge is to enable accurate, fast simulation using real-world models, without slowing down the engineering team.

> "The customer gives us the semiconductor wafers from TSMC or Global Foundries or Samsung. Then we do wafer bumping, sorting, package design, electrical and thermal simulations. We next tape out the package, manufacture the substrate, do the assembly and final test. We send the customer assembled packages to do their lab evaluation, and ultimately ship the product."
>
> **Larry Zu**

Initially, Sarcina tried industry-standard SPICE-based simulation tools. The company immediately encountered difficulty: lack of good user interfaces among tools, and the need for a lot of text-based model configuration. Sarcina's engineers wanted a tool that would focus more on the task at hand and maintain model accuracy without getting bogged down in scripting.

Accuracy is critically important for simulation of chip packages and essential for achieving first-time package tape-out success. Accurate simulation of chip packages and the PCB channel is necessary for feeding back Signal Integrity / Power Integrity (SI/PI) performance into design changes that make the system work within the necessary margins.

Most of the cost of package design lies in required multiple engineering disciplines: layout, manufacturing, signal and power integrity, EMC, and test. Simulation traditionally has been the bottleneck to getting package designs finalized and ready for production, in large part due to extended simulation runs that consume days of computing. Sarcina needed an EDA tool that would accelerate simulation and provide their engineers overnight results.

Due to the cutting-edge nature of package design around new (unreleased) silicon, signal speeds, and voltage levels are being used which have not been used before. It's therefore necessary to be able to integrate additional model and parameter extraction methods and tools, using the resulting data in the main simulator without having to modify it. Moreover, it's desirable to have the ability to create brand-new models based upon the silicon designer's input.

Solution: End-to-end workflow for productivity

Sarcina developed a detailed workflow for end-to-end package design services, centered around simulation. Traditional package and interconnect designers tend to only address signal integrity at the PCB level, but by adopting ADS and the multi-model signal path approach, Sarcina's results accurately represent the real-world signal characteristics. ADS is the backbone of this workflow for simulation because it is the easiest to use and most accurate for such complex tasks. Power Integrity is also challenging in such small areas where power dissipation can be hundreds of watts (Figure 1).

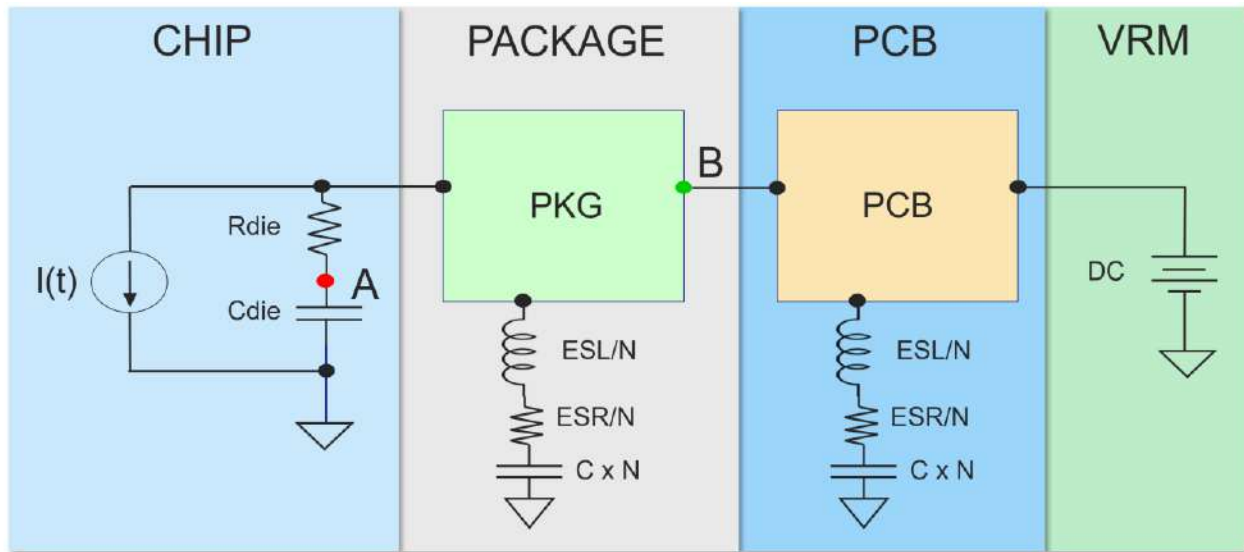

Figure 1. End-to-End PI analysis

"You know, at 54 Gbps data rate and with bi-directional simulation, we can validate not only the silicon but also the package and the PCB."

Larry Zu

To accurately simulate an entire channel, the physical layout of the package signal paths, connectors, and PCB traces are all extracted using a 3D electromagnetic solver. The resulting frequency domain S-Parameter files are then used to precisely replicate the transfer function of each critical signal path. ADS uses S-Parameters with great efficiency by converting S-Parameter files into time domain impulse response (IR) coefficients, which are convolved with the input stimulus during simulation.

Accurate simulation requires covering the entire channel, as depicted in Figure 2. This example demonstrates DDR channel simulation that involves several interconnect structures which normally introduce reflections and crosstalk. By simulation of the entire end-to-end channel, Sarcina is able to pinpoint every location in the package design that must be modified to reduce impedance discontinuities.

Six years ago, Sarcina developed a cost-effective package for a network processor. Multiple channels had to be designed fitting 20 SerDes lanes, 8 PCIe Gen 3 lanes, and 3733 MT/s 32-bit LPDDR4 – all into a 23mm x 23mm 480-ball FCBGA package. This required the package to have a 2-2-2 layer stack. This is

no easy task given that the package also must include enough capacitance on-board to meet power integrity requirements.

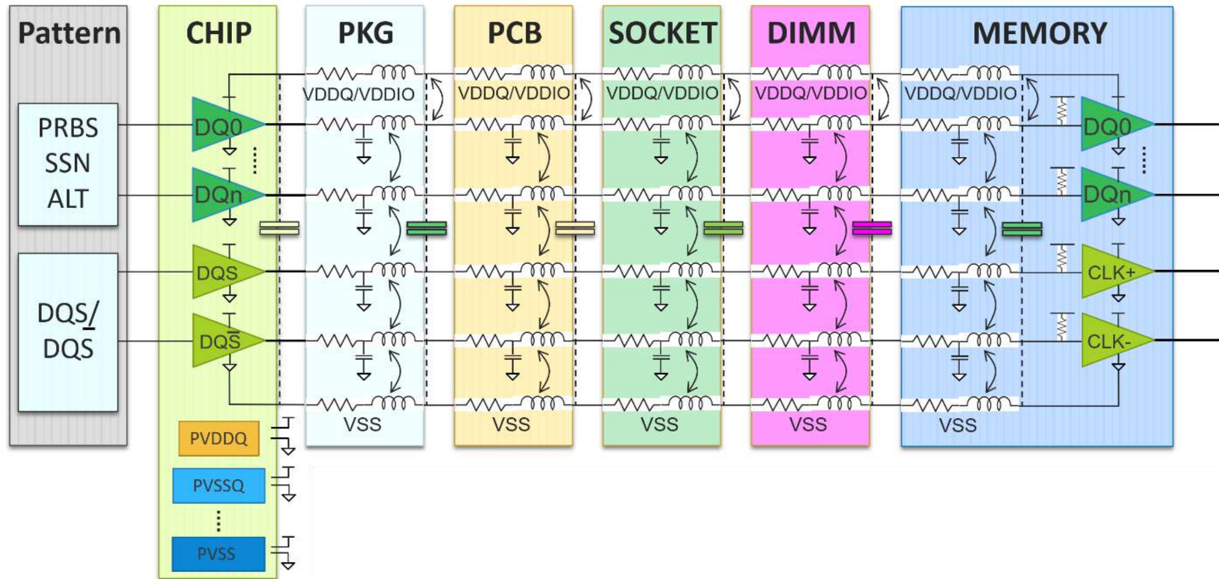

Figure 2. LPDDR5 detailed channel analysis schema

To achieve first-time success, Sarcina uses Keysight ADS along with:

- IBIS-AMI models of new silicon provided by the IP Vendor
- S-parameter EM extractions from the package substrate and routing
- Transient PRBS (Pseudo-Random Bit Sequence) and DC simulation sources

Design requirements are provided in terms of allowable channel loss vs frequency, voltage high and low levels, BER (Bit Error Rate), and power supply tolerance (Figure 3). Sarcina uses this as input to configure ADS for SI/PI simulation, as well as output graph generation and pass/fail analysis.

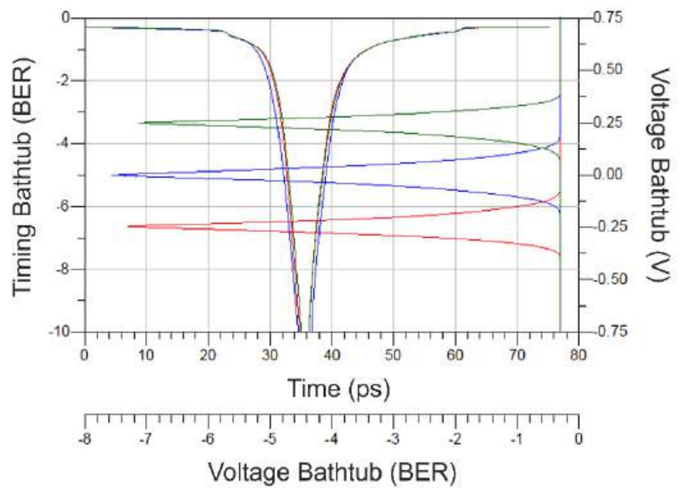

Figure 3. BER requirements overlayed on voltage bathtub

In high-speed digital systems, multi-level signaling increases throughput on lossy PCB and package substrates without increasing the Nyquist frequency (symbol rate). Standards like PCIe Gen 6 and 100 Gbps Ethernet all require this and adopt PAM4 (Phase/Amplitude Modulation, 4-Level). PAM4 offers the best currently available data throughput within signal-to-noise ratio (SNR) and channel loss budgets.

Sarcina designs packages for the latest semiconductors and employs ADS with the latest IBIS-AMI models and signal sources. Using the built-in simulation libraries and models from the semiconductor IP vendors, they integrate modern high-speed modulated signaling. This enables accurate results, and a clear view as to how package design elements (as shown in Figure 4) physically impact modulation and can cause issues such as unbalanced eyes, offset, SNR, and jitter.

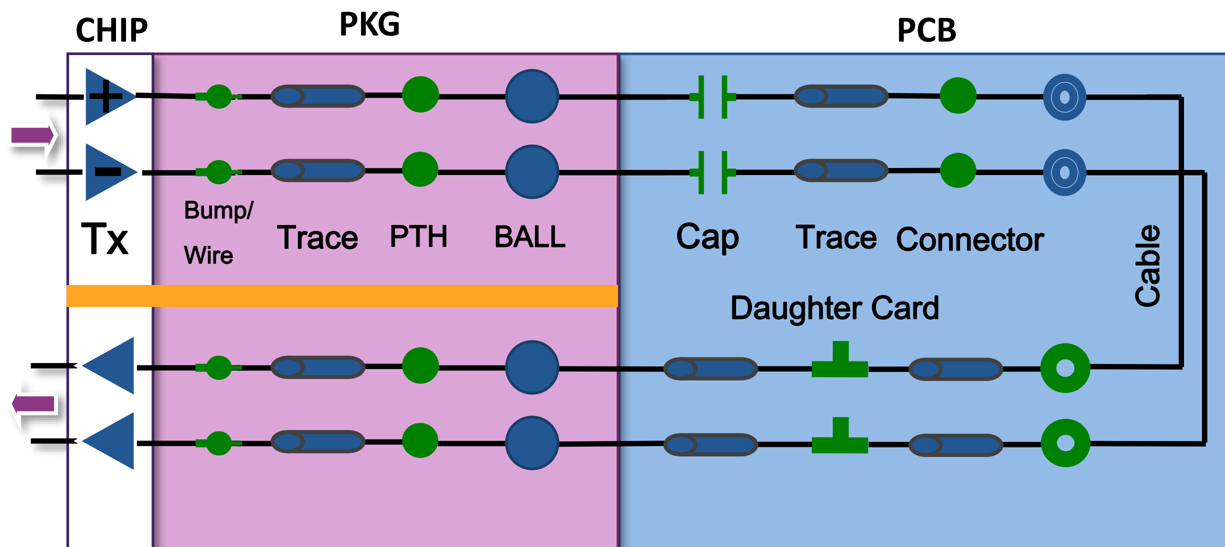

Figure 4. 56 Gb/s PAM4 topology of Network Processor

Sarcina selected Keysight ADS as their central simulation tool. Their engineering team evaluated alternatives and made a unanimous decision based on productivity.

> "The engineers love the interface, the ease-of-use of ADS."
>
> **Larry Zu**

The Sarcina team wanted a system that had an intuitive graphical user interface with rich model libraries. The block-based design approach, with each item in the signal chain being configurable through wizards and dialogs that are designed with the end user in mind, made the team productive immediately. ADS came out on top for performance, accuracy, and ease of use.

> "Based on the scale of our simulations, getting convergence can be a big challenge. We're not just simulating a few components. We're dealing with hundreds of components, so the accuracy, and resolving SPICE convergence issues are very important."
>
> **Larry Zu**

Results: Simulation matches measurements

Sarcina has a 100% success rate for all of the package designs using ADS at the heart of their workflow. Accuracy is particularly important and includes every element of the signal and power distribution network on each package.

Traditional loadboard design analysis focuses on PCB layout, but fails to include package, connector, and cable effects. ADS allows easy integration of the entire signal chain, including external component S-Parameter and IBIS-AMI models. This allowed Sarcina to accurately test the entire system before committing the loadboard design to manufacturing.

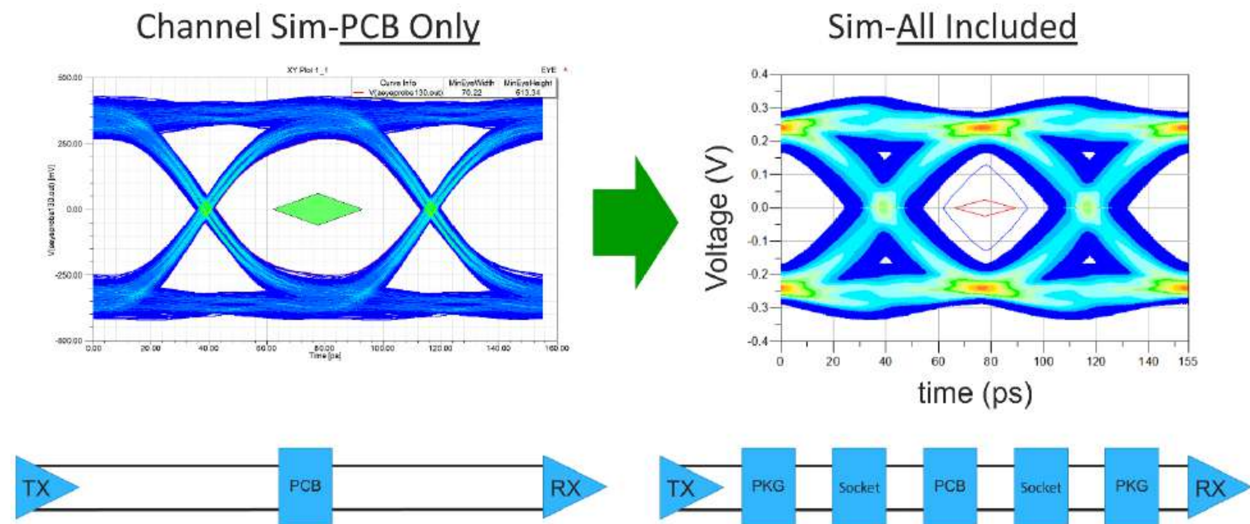

Figure 5. Simulation accuracy afforded by ADS

Figure 5 compares the ADS simulation results. This compares favorably to the measurement on Keysight instruments in the customer's lab. The ADS simulation, when set up with the right parameters and models, produces results that correlate very precisely with real-world measurements.

Another example case is a high-speed NPU. Sarcina created an advanced package design that utilized 6400 MT/s LPDDR5 memory. Configuring the package layer stack, power and ground references, and routing according to the electrical requirements, enabled Sarcina to create a first-time success with a very demanding signaling scheme in a fraction of the time it would take using other tools (Figure 6).

> “We did a measurement with Keysight test equipment. We captured an eye diagram from the measured computer screen and compared it against the simulation result. We positioned them one on top of each other and they were practically identical.”
>
> **Larry Zu**

6400 Mb/s LPDDR5 Channel Simulation

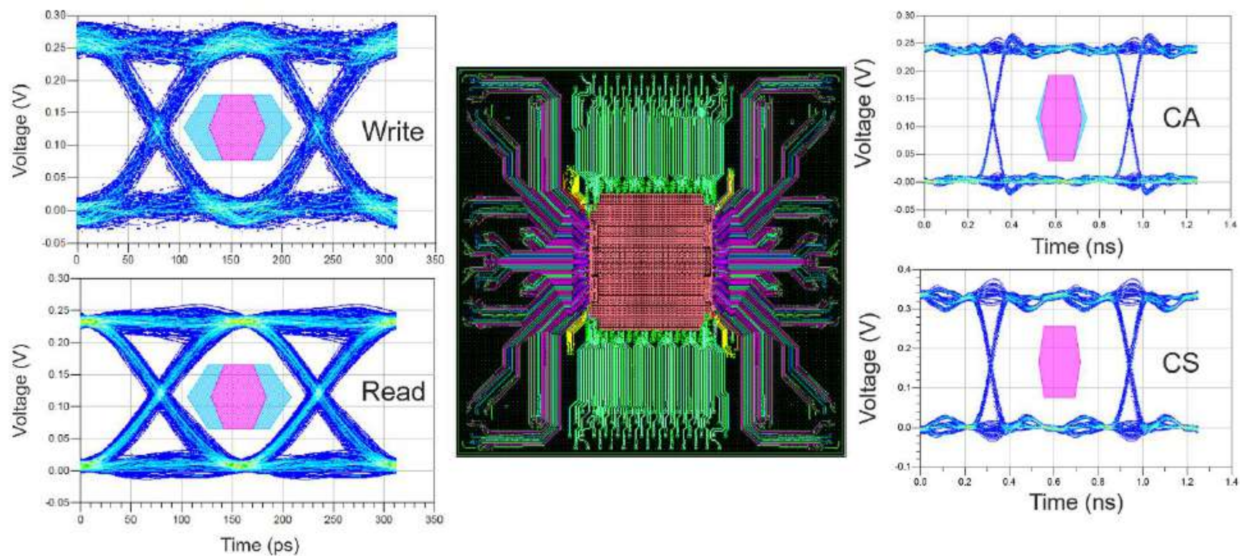

Figure 6. Results of LPDDR5 SI with network processor

By importing cutting-edge IBIS-AMI models from silicon IP vendors, Sarcina performed accurate bi-directional analysis on the LPDDR5 interconnects. Different devices on the interconnect have different signal drive strengths. The results of performing these simulations in Keysight ADS and Memory Designer show that with the correct driver and termination settings for the die, signal integrity across the package is maintained and there is plenty of eye margin.

> “We heavily rely on ADS and Memory Designer simulation results to give us a hint as to design change direction.”
>
> **Larry Zu**

Another case cited by Sarcina is 56 Gbps Ethernet, consisting of two differential channels paired and using PAM4 modulation.

Using the customer's requirements, Sarcina specifies the eye contours for channel simulation that yield bit error rate (BER) demands. Figure 7 shows the eye contour created in ADS that met the specified targeted performance. The graph is the simulation result after 1.5 million bits of PAM4 PRBS data were simulated.

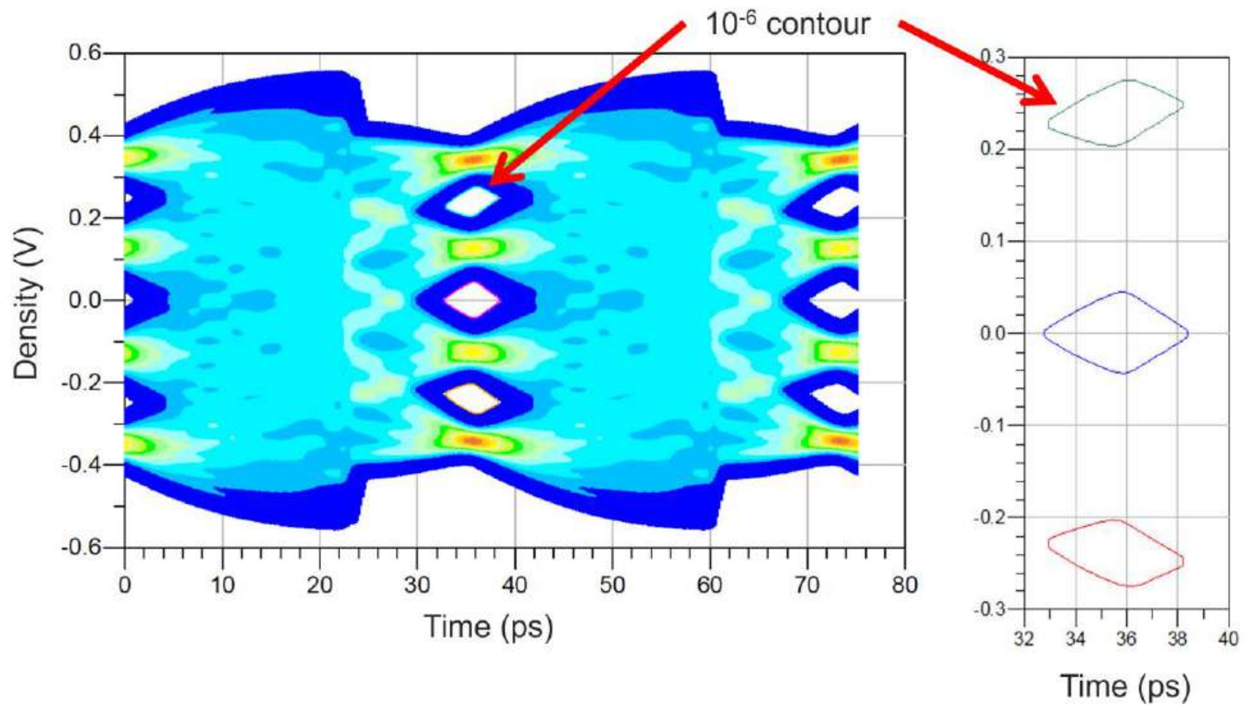

Figure 7. PAM4 eye masks for 56 Gb/s channel

Sarcina saves cost

By integrating ADS and Memory Designer into the complete package design, simulation, die-bond, and bring-up test workflows, Sarcina specializes in this unique and difficult task.

Some semiconductor start-ups hire their own packing engineering staffs. While this can work well for simpler devices, more often than not, fabless semiconductor start-ups do not have the skill set or resources to take on the challenge.

A typical packaging team includes a power integrity simulation engineer, a signal integrity simulation engineer, a package layout engineer, a manager to manage the team with knowledge and experience in this niche, and close relationships with two packaging factories to mitigate supply chain risk. Sometimes, a thermal/mechanical engineer and an assembly process engineer are also needed.

The annual cost for this team, including human resources and software, is close to $2 million . Although the cost in China drops to $1 million, it's not financially possible to support such a team because start-ups usually tape out only one chip every two years. In other words, the team would be idle more than half the time.

Sarcina, however, accomplishes the job with a fraction of the budget, saving hundreds of thousands of dollars for every advanced package.

Learn more about Sarcina's advanced packaging design services at: https://sarcinatech.com/

For more information about Keysight simulation solutions, please visit:

PathWave Advanced Design System (ADS)

PathWave SIPro

PathWave PIPro

PathWave Memory Designer

PathWave Advanced DDR AMI Modeler

All figures courtesy of Sarcina Technology.

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