OUR COMPANY

When Sarcina Technology opened for business in 2011, it laid the foundation for an evolving link in the semiconductor industry value chain … the Application Specific Advanced Packaging (ASAP) Services.

Hyper-performance semiconductor companies demand high-performing packaging and test capability tuned to very specific product-driven specs. But they also want assign-it-and-forget-it dependability and high cost-to-value return. Off-the-shelf, standard semiconductor packaging clearly won't cut it.

Sarcina built the ASAP category by providing dependable, creative, and assured advanced package design, test, assembly, and production management services and a 100 percent first-time silicon success track record.

TECHNOLOGY

As advanced technology node cost skyrockets and higher performance ASIC demand increases, multi-die chiplet packaging extends Moore's Law. At the same time, ASICs have extended their reach into new territories such as space, automotive, photonics and biomedical devices. Sarcina designs ASIC packages in all these segments for top-tier semiconductor, IT, and system companies.

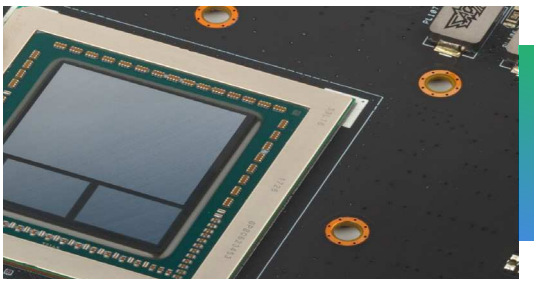
PACKAGING

Sarcina has designed over 100 advanced packages including:

- 2.5D Silicon Interposer Packaging
- 3D Packaging
- Multi Chip Module/Chiplet Packaging
- Photonic IC Packaging
- Automotive Packaging

Sarcina has also built a reputation for cost-effective, high yield standard packaging including:

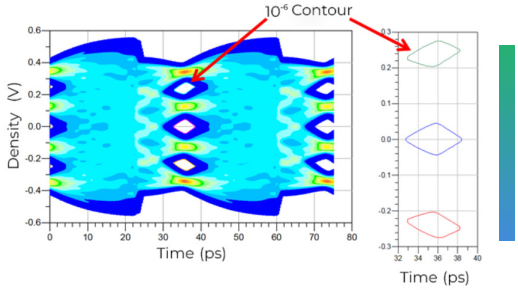
- Flip-Chip BGA Packaging
- Wirebond BGA Packaging
- QFN Packaging



SIMULATION

Sarcina conducts rigorous channel simulation to validate package design before tape-out. Analysis includes power integrity simulation with chip-package-PCB, signal integrity eye-diagram channel simulation for high speed I/O, and system thermal simulation with detailed die and package models to accurately predict silicon junction temperature. Simulation services cover:

- Power delivery network simulation
- LPDDR5/DDR5/GDDR6 channel simulation
- SerDes channel simulation
- PCIe channel simulation
- System thermal simulation



TESTING

Sarcina stays ahead of the industry's test hardware development curve. It not only designs and simulates advanced packages, but also utilizes these capabilities to develop state-of-the art production test hardware.

SERVICES

Sarcina provides a complete semiconductor packaging service portfolio for emerging companies in the hyper performance semiconductor market demand state of the art packaging/test services that deliver very specific product driven specs. At the same time, they want assign-it-and-forget-it dependability and high cost-to-value return.

WIPO INTEGRATED SERVICE

Lower total packaging costs with Sarcina's exclusive WIPO service. WIPO stands for wafer-in, product-out and it eliminates the exorbitant costs of maintaining a hardware team for packaging, testing, and production. WIPO covers: wafer bumping, wafer sort, package design, test hardware design, design simulations, substrate/hardware fabrication, chip assembly, final test, device qualification, and production.

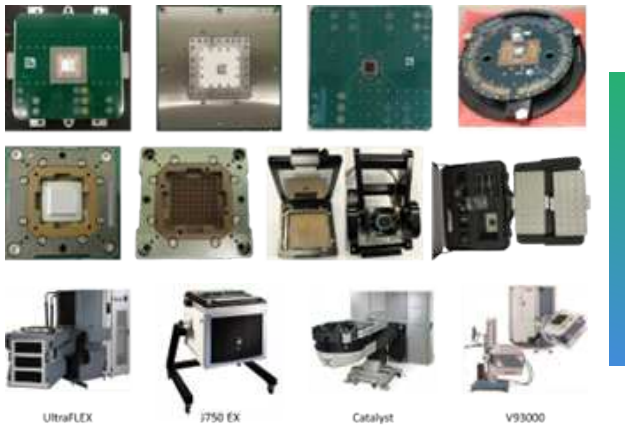
PACKAGING SERVICES

Sarcina provides a complete semiconductor packaging service portfolio.

- Package Selection
- Package Design
- Power Integrity/Signal Integrity Simulation
- Thermal Simulation
- Substrate Fabrication
- Package Assembly

TESTING SERVICES

Sarcina's one-stop testing service starts with a test plan. We then design, manufacture, and assemble all the testing hardware, including wafer sort probe cards, final test loadboards, sockets, change kits, and layout kits for Automatic Test Equipment (ATE). Customers provide DFT test patterns that Sarcina converts to executable ATE testing files. During final test and/or wafer sort, Sarcina customizes each customer's work flow to seamlessly ramp to production.



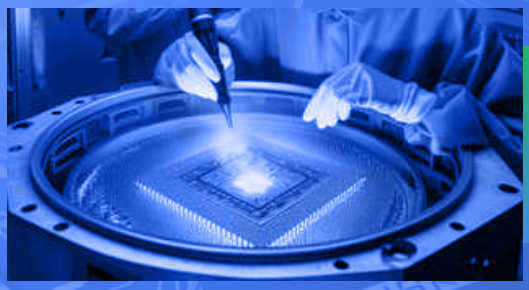
Sarcina testing hardware and tester selections

QUALIFICATION SERVICES

Sarcina offers two qualification services:

- High Temperature Operating Life (HTOL) for IC qualification on burn-in-board (BIB)
- Package qualification

Both follow the JEDEC standard



PRODUCTION MANAGEMENT SERVICES

Sarcina production management services reduce engineering overhead and speed time-to-volume. Services cover yield enhancement, wafer bumping, wafer sort, assembly, final testing, failure analysis, return material authorization, and logistics order and shipping.

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